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FORM: PTO-1449 (REV: 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Atty Docket No: 95-0653.02	Serial No: 08/984,562
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b)) (use several sheets if necessary)		Applicant: Mailloux et al.	
		Filing Date: December 3, 1997	Group: 2751

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass
Wh	AA	5,357,469	10/18/94	Soimmer et al.	365 193
↑	AB	5,268,865	12/7/93	Takasugi	365 189.5
↑	AC	4,618,947	10/21/86	Tran et al.	365 230 236
↑	AD	5,267,200	11/30/93	Tobita	365 189.5 189.05
↑	AE	4,344,156	8/10/82	Eaton et al.	365 203 189.05
↑	AF	4,707,811	11/17/87	Takemae et al.	365 239
↑	AG	4,649,522	3/10/87	Kirsch	365 189.05
↑	AH	4,603,403	7/29/86	Toda	365 189.05
↑	AI	4,567,579	1/28/86	Patel et al.	365 189.05
↓	AJ	4,484,308	11/20/84	Lewandowski et al.	365 711 900 109
Wh	AK	4,875,192	10/17/89	Matsumoto	365 193

FOREIGN PATENT DOCUMENTS

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Initial

OTHER ART (including author, title, date, pertinent pages, etc.)

Wh	AR		Samsung Electronics, "Samsung Synchronous DRAM", March 1993, pgs. 1-16
Wh	AS		Oki Electric Ind. Co., Ltd., "Burst DRAM Function & Pinout", 2nd presentation, Item #619, September, 1994 <i>duplicate see para #4</i>
Wh	AT		Toshiba, "Pipelined Burst DRAM", December 1994, JEDEC JC-42.3 Hawaii

Examiner: H. Kim	Date Considered: 4/2/99
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U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	
Wk	AA	4,685,089	8/4/87	Patel et al.	365	233,189.05
↑	AB	4,562,555	12/31/85	Ouchi et al.	365	233,189.03
	AC	4,575,825	3/11/86	Ozaki et al.	365	189,193
	AD	4,788,667	11/29/88	Nakano	365	193
	AE	5,392,239	2/21/95	Margulis et al.	365	189,01
	AF	5,379,261	1/3/95	Jones, Jr.	365	230.01
	AG	5,126,975	6/30/92	Handy et al.	365	230.01
	↓	AH	5,331,593	7/94	Merritt	365
	AI	5,311,471	5/90	Matsumoto	365	189.05
Wk	AJ	5,526,320	6/11/96	Zagar et al.	365	233.5

FOREIGN PATENT DOCUMENTS

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OTHER ART (including author, title, date, pertinent pages, etc.)

Wk	AR		Toshiba America Electronic Components, Inc., "Application Specific DRAM, 1994", Pgs. C-178, C-260, C218
Wk	AS		Micron Semiconductor, Inc., "Synchronous DRAM 2 MEG x 8 SDRAM", Pgs. 2-3 through 2-6, Rev. 4/94
Wk	AT		Toshiba America Electronic Components, Inc., "4M DRAM 1991", Pgs. A-137 - A-159

Examiner: <u>H. Korn</u>	Date Considered: <u>4/2/99</u>
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U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass
ML	AA 5,268,865	12/93	Takasugi	365	189.05
↑	AB 5,319,759	6/94	Chan	365 711	230.08 217
↑	AC 5,327,390	7/94	Takasugi	365	230.08 230.06
↑	AD 5,426,606	6/95	Takai	365	230.06 189.05
↑	AE 5,369,622	11/94	McLaury	365	233
ML	AF 5,568,445	10/96	Park et al.	365	233
↑	AG 5,652,724	7/97	Manning	365	189.05
↑	AH 5,610,864	3/97	Manning	365	193
↑	AI 5,526,320	6/96	Zagar et al.	365	233.5
↑	AJ 5,392,239	2/95	Margulis et al.	365	189.01
ML	AK 5,175,835	12/92	Beighe et al.	711	212

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Duplicate see paper No 4
PTO-742**OTHER ART** (including author, title, date, pertinent pages, etc.)

ML	AR		Micron Semiconductor, Inc., "1994 DRAM Data Book", pgs. 2-1 to 2-6
ML	AS		Mosel-Vitellic V53C8257H DRAM Specification Sheet, 20 pgs.
ML	AT		Toshiba Corp., "Integrated Circuit Technical Data-262,144 Words x 8 Bits Multiport DRAM", TC52826TS/Z/FT/TR, TEN. Rev. 2.1

Examiner: H. Kim	Date Considered: 4/2/99
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U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	
<i>Wk</i>	AA 5,146,582	9/92	Begun	395	280 500	<i>Sept 1992</i>
<i>Wk</i>	AB 4,851,990	7/89	Johnson et al.	395 710	280 100	
<i>Wk</i>	AC 4,519,028	5/85	Olsen et al.	395	559	
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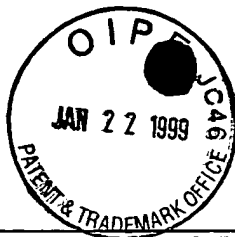
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OTHER ART (including author, title, date, pertinent pages, etc.)

<i>Wk</i>	AR		Micron Technology, Inc., "Burst EDO DRAM Information", pgs. 1-126, Rev. 9/95
<i>Wk</i>	AS		NEC "Command Truth Table" March 15, 1993
<i>Wk</i>	AT		Samsung Electronics "KM48SV2000 Preliminary CMOS SDRAM" Rev.1(Mar, 1993), pgs. 7-8

Examiner: <i>H. Kim</i>	Date Considered: <i>4/2/99</i>
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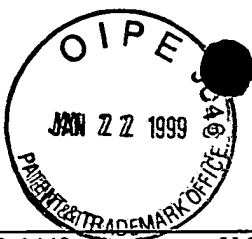
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OTHER ART (including author, title, date, pertinent pages, etc.)

Initial			
	AR		S3 Incorporated, "S3 Burst Mode DRAM", 6/93, 2 pages
			<i>duplicate</i>
	AS		Electronic News "Mitsubishi Samples 16M Synch DRAM", 10/25/93, pgs. 3-4
	AT		"DRAM 1 Meg X 4 DRAM 5BEDO Page Mode", 1995 DRAM Data Book, pp.1-1 thru 1-30,, (Micron Technology, I)

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Initial

OTHER ART (including author, title, date, pertinent pages, etc.)

<i>Wk</i>	AR		"Hyper Page Mode DRAM", 8029 Electronic Engineering, 66, No. 813, Woolwich, London, GB, pp. 47-48, (September 1994)
<i>Wk</i>	AS		Dave Bursky, "Novel I/O Options and Innovative Architectures Let DRAMs Achieve SRAM Performance; Fast DRAMS can be swapped for SRAM Caches", Electronic Design, Vol. 41, No. 15, Cleveland, Ohio, pp. 55-67, (July 22, 1993)
<i>Wk</i>	AT		Shiva P. Gowni, et al., "A 9NS, 32K X 9, BICMOS TTL Synchronous Cache RAM With Burst Mode Access", IEEE, Cutsom Integrated Circuits Conference, pp. 781-786, (March 3, 1992)

Examiner: <i>Kh Korn</i>	Date Considered: <i>4/2/99</i>
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Wk	AR		Micron Semiconductor, Inc., "Synchronous DRAM 4 Meg x 4 SDRAM", Pgs. 2-1 to 2-2
Wk	AS		Micron Technology, Inc., "1996 DRAM Data Book", Pgs. 1-1 to 1-52, and 4-1 to 4-42
Wk	AT		Micron Technology, Inc., "1995 DRAM Data Book", Pgs. 3-1 to 3-37

Examiner: H Kim	Date Considered: 4/2/99
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Initial

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See AR		Performance; Fast DRAMS can be swapped for SRAM Caches", Electronic Design, Vol. 41, No. 15, Cleveland, Ohio, pp. 55-67, (July 22, 1993)
See AR		Access", IEEE, Custom Integrated Circuits Conference, pp. 781-786, (March 3, 1992)
See AR		S3 Incorporated, "S3 Burst Mode DRAM", 6/93, 2 pages
See AR		Micron Technology, Inc., "1995 DRAM Data Book" pp. 4-1 thru 4-42, 12/95.
AT		dupl onl see paper 4 pTO-892

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